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10/815,604	03/31/2004	Andrew Ho	RA290.CIP1US	1158
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SILICON EDGE LAW GROUP, LLP			PERILLA, JASON M	
6601 KOLL CENTER PARKWAY				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/815,604	HO ET AL.	
Examiner	Art Unit		
Jason M. Perilla	2611		

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 09 October 2007.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-8, 10-14, 16-25, 27-36, 38-43, 45 and 46 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 1-8, 10 and 11 is/are allowed.

6) Claim(s) 12-14, 16-25, 27-30, 34-36 and 40-43 is/are rejected.

7) Claim(s) 31, 32, 33, 38-39, and 45-46 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 31 March 2004 is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date. _____
3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ 5) Notice of Informal Patent Application _____
6) Other: _____

DETAILED ACTION

1. Claims 1-8, 10-14, 16-25, 27-36, 38-43, 45, and 46 are pending in the instant application.

Response to Amendment/Argument

2. The Applicant's claim amendments and arguments filed October 9, 2007 have been considered by the Examiner.

- a. Regarding the drawings: The Applicant's remarks are not persuasive. The drawings do not illustrate the claimed subject matter. With respect to the features of claim 3, the Applicant suggests that the specification describes the claimed features and that the drawings are in accordance with the specification. However, claims 1 and 3 provide that the first and second samplers output first and second sampled data streams and the "comparison circuit is adapted to compare *at least one of the sampled-data streams* with expected data." Therefore, the drawings must show (1) a comparator, (2) two sampled data streams, and (3) expected data. Furthermore, the drawings must illustrate the comparator being operatively able to compare either one of the first or second data streams with the expected data via the comparator. Presently, no drawings illustrate the claimed subject matter.
- b. Regarding the arguments against the prior art combination of Matsumoto et al (U.S. Pub. No. 2002/0131531; "Matsumoto") in view of Lee et al (U.S. Pub. No. 2002/0085656; "Lee"), they are not persuasive. Clarified arguments are set forth below.

Drawings

3. The drawings are objected to under 37 CFR § 1.83(a) because they fail to show the following:

c. The features of claim 3. Specifically, none of the drawings show the "comparison circuit" of claim 1 having first and second input terminals respectively coupled to the outputs of first and second samplers as well as having (supposedly) a third input to compare at least one of the sampled data streams with expected data as limited in claim 3. Rather, figure 4 is the only figure illustrating a comparator (430) comparing a sampler (405) output with expectation data (425). However, figure 4 is an alternative embodiment outside the scope of parent claim 1.

Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR § 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each

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drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 12, 13, 16-19, 21, 23, 24, 26, 27, 34, 40-43 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsumoto et al (U.S. Pub. No. 2002/0131531; "Matsumoto" – previously cited) in view of Lee et al (U.S. Pub. No. 2002/0085656; "Lee" – previously cited).

Regarding claim 12, Matsumoto discloses, according to figure 2) a method comprising: a. sampling a series of input symbols ("INPUT DATA SIGNAL") using a first clock signal of a first clock phase ("CLK") to produce a first series of sampled symbols (output of 120b); b. sampling the series of input symbols using the first clock signal of a first clock phase to produce a second series of sampled symbols (output of 120a); and c. comparing (fig. 2, ref. 130a) sampled symbols of the first series of sampled symbols with corresponding sampled symbols of the second series of sampled symbols; wherein the series of input symbols are sampled using the first clock phase at a first sample

voltage ("V_{th}") and using the first clock phase at a second sample voltage ("V_m"). Matsumoto discloses two samplers (110a & 120a, and 110b & 120b) each receiving an input data signal and the same clock signal ("CLK") but does not disclose that each sampler receives a respective clock signal (i.e. first and second clock signals). However, Lee discloses a strictly analogous data recovery receive circuit wherein each of a plurality of samplers (fig. 5, refs. 502-504) receive a respective clock signal (fig. 5, refs. 414-416). Lee teaches that the use of independent clock signals permits the generation of the "desired three phase clocks" which may have independent phases (¶ 0030). Using the various phases permits the determination of a data "edge" as is notoriously known in the art. That is, the multiple phases permit the determination of where the data changes from one state to another (i.e. state or edge change). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to apply phase independent clocks to each respective sampler of Matsumoto as taught by Lee because it would permit more flexibility in the reception and analysis of the input data by permitting the detection of data edges.

Regarding claim 13, Matsumoto in view of Lee disclose the limitations of claim 12 as applied above. Further, in the combination of Matsumoto in view of Lee, it is clear that Lee's teaching imparts adjusting, in response to the comparing, at least one of the first and second clock phases with respect to the other of the first and second clock phases. The phase adjustment is made to the timing between phases "TM" (see fig. 310; ¶¶ 0028 & 0033).

Regarding claim 16, Matsumoto in view of Lee disclose the limitations of claim 15 as applied above. Further, Matsumoto discloses adjusting (fig. 2, ref. 10) at least one of the first and second sample voltages with respect to the other of the first and second sample voltages in response to the comparing (fig. 2, "H LEVEL ERROR PULSE" and "L LEVEL ERROR PULSE").

Regarding claim 17, Matsumoto in view of Lee disclose the limitations of claim 12 as applied above. Further, Matsumoto discloses issuing an error signal (fig. 2, "H LEVEL ERROR PULSE") in response to a mismatch between ones of the first and second series of sampled symbols.

Regarding claim 18, Matsumoto in view of Lee disclose the limitations of claim 12 as applied above. Further, Matsumoto discloses that comparing produces error data for a plurality of phase offsets between the first and second clock phases (fig. 2, "H LEVEL ERROR PULSE" and "L LEVEL ERROR PULSE"), the method further comprising storing the error data (fig. 4). In the combination of Matsumoto in view of Lee, the phase offsets will vary according to Lee's phase controller (fig. 4, ref. 410) and phase shifter circuits (fig. 4, ref. 413). Therefore, as broadly as claimed, Matsumoro in view of Lee's circuitry will produce error data for a plurality of phase offsets. Furthermore, Matsumoto's "DECISION THRESHOLD VOLTAGE CONTROL CIRCUIT" (fig. 2, ref. 10) would store the plurality of error signals according to the flow diagram of figure 4.

Regarding claim 19, Matsumoto in view of Lee disclose the limitations of claim 18 as applied above. Further, Matsumoto discloses storing information regarding each of the phase offsets and the corresponding error data as applied in claim 18 above.

Regarding claim 21, Matsumoto in view of Lee disclose the limitations of claim 18 as applied above. Further, Matsumoto in view of Lee disclose that the series of input symbols are sampled using the first clock phase (i.e. Lee; fig. 4, ref. 414) at a first sample voltage (Matsumoto; fig. 2, "Vm") and using the second clock phase (i.e. Lee; fig. 4, ref. 415) at a second sample voltage (Matsumoto; fig. 2, "Vth"), and wherein the comparing produces second error data (Matsumoto; fig. 2, "H LEVEL ERROR PULSE") for a plurality of voltage offsets between the first and second sample voltages. See also, discussion of the operation of Matsumoto in view of Lee in claim 20 below.

Regarding claim 23, Matsumoto in view of Lee disclose the limitations the claim as applied to claim 12 above.

Regarding claim 24, Matsumoto in view of Lee disclose the limitations of claim 23 as applied above. Further, Matsumoto discloses adjusting (fig. 2, ref. 10) at least one of the first and second sample voltages with respect to the other of the first and second sample voltages in response to the comparing (fig. 2, "H LEVEL ERROR PULSE" and "L LEVEL ERROR PULSE").

Regarding claim 26, Matsumoto in view of Lee disclose the limitations of claim 23 as applied above. Further, Matsumoto in view of Lee disclose that the series of input symbols are sampled using a first clock phase (i.e. Lee; fig. 4, ref. 414) and a second clock phase (i.e. Lee, fig. 4, ref. 415).

Regarding claim 27, Matsumoto in view of Lee disclose the limitations of claim 23 as applied above. Further, Lee discloses the remaining limitations of the claim as applied to claim 13 above.

Regarding claim 34, Matsumoto in view of Lee disclose the limitations of the claim as applied to claim 12 above. Further, Matsumoto discloses a transmitter to transmit signals (fig. 2, "AMP").

Regarding claim 40, Matsumoto in view of Lee disclose the limitations of the claim as applied to claim 12 above.

Regarding claim 41, Matsumoto in view of Lee disclose the limitations of claim 40 as applied above. Further, Matsumoto discloses that the first and second sampling means respectively produce sampled data streams as applied to claim 1 above.

Regarding claim 42, Matsumoto in view of Lee disclose the limitations of claim 41 as disclosed above. Furthermore Matsumoto discloses that the comparison circuit (fig. 2, ref. 130a) issues an error signal ("H LEVEL ERROR PULSE") in response to mismatches between the first and second sampled-data streams.

Regarding claim 43, Matsumoto in view of Lee disclose the limitations of claim 42 as applied above. Further, Matsumoto discloses the remaining limitations of the claim as applied in claim 42 above.

6. Claims 14, 25, 35, and 36 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsumoto in view of Lee, and Best et al (U.S. Pub. No. 2002/0196883 – previously cited).

Regarding claim 14, Matsumoto in view of Lee disclose the limitations of claim 12 as applied above. Matsumoto in view of Lee do not explicitly disclose that the data input terminal, the first sampler, the second sampler, and the comparison circuit are disposed on a semiconductor chip. However, placing several circuit components on a

single semiconductor substrate is notoriously known in the art as evidenced by Best (¶ 0047). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the various circuit components of Matsumoto in view of Lee could be disposed on a single semiconductor chip or integrated circuit as disclosed by Best.

Regarding claim 25, Matsumoto in view of Lee disclose the limitations of claim 23 as applied above. Further, Best discloses the remaining limitations of the claim as applied in claim 2 above.

Regarding claim 35, Matsumoto in view of Lee disclose the limitations of claim 34 as applied above. Further, Best discloses the remaining limitations of the claim as applied in claim 2 above.

Regarding claim 36, Matsumoto in view of Lee, and in further view of Best disclose the limitations of claim 35 as applied above. Matsumoto in view of Lee, and in further view of Best do not explicitly disclose that the transmitter is disposed on a second semiconductor chip. However, as notoriously understood by one having ordinary skill in the art, various circuits may be disposed upon a single or multiple semiconductor chips. Circuits disclosed upon multiple semiconductor chips may be interconnected using printed circuit boards, for instance. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the transmitter could be disposed upon a second semiconductor chip because placing circuits on various semiconductor chips and connecting them using circuit boards is well known and accepted in the art.

7. Claim 20, 22, 28, 29 and 30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsumoto in view of Lee, and Tobias et al (U.S. Pat. No. 7188261 – previously cited).

Regarding claim 20, Matsumoto in view of Lee disclose the limitations of claim 18 as applied above. Specifically, in the original circuit of Matsumoto (fig. 2), the control circuit (10) determined the errors among sampling positions against variable voltage threshold levels (fig. 2, V_m , V_{th} , and V_s and fig. 6). Matsumoto's control circuit (fig. 2, ref. 10) performed an analysis upon (figs. 4 and 5) stored error signals attributable to the various threshold voltages. Figures 6 and 7 represent "schmoos" of these errors by the control circuit 10. In the combination of Matsumoto in view of Lee, both the voltage thresholds (Matsumoto; fig. 2, V_m , V_{th} , and V_s) and the phases of sampling clocks (i.e. Lee, fig. 4, refs. 414-416 replacing Matsumoto's fig. 2, "CLK") are variable. Each is stored in the control circuit (fig. 2, ref. 10) of Matsumoto for analysis.

Further regarding claim 20, although Matsumoto in view of Lee have the ability to "calculate a timing margin" or schmoo the characteristics of the data samples against both the voltage thresholds and the variable phase timings, the calculation of a timing margin is not explicitly disclosed by Matsumoto in view of Lee. However, Tobias discloses calculating a timing margin or "identifying usable operational set points in a schmoo plot" (fig. 6B, ref. 624). Therefore it would have been obvious to one skilled in the art to utilize the circuitry of Matsumoto in view of Lee to calculate a timing margin by reading a schmoo plot (Tobias; fig. 6B, ref. 622) and identifying a timing margin as

taught by Tobias because it could be utilized to determine a circuits margin against its own operational specifications.

Regarding claim 22, Matsumoto in view of Lee disclose the limitations of claim 21 as applied above. Further, in the schmoo of Matsumoto in view of Lee, and in further view of Tobias as applied according to claim 20 above, the combination discloses plotting the first-mentioned error data (threshold voltages) against the second error data (phase timings).

Regarding claim 28, Matsumoto in view of Lee disclose the limitations of claim 27 as applied above. Further, Matsumoto in view of Lee, and in further view of Tobias disclose storing information regarding the first and second sample voltages and the first and second clock phases as applied in claim 20 above.

Regarding claim 29, Matsumoto in view of Lee disclose the limitations of claim 28 as applied above. Further, Matsumoto in view of Lee, and in further view of Tobias disclose calculating a timing margin as applied in claim 20 above.

Regarding claim 30, Matsumoto in view of Lee disclose the limitations of claim 28 as applied above. Further, Matsumoto in view of Lee, and in further view of Tobias disclose plotting the information (Tobias; fig. 6A, ref. 602; fig. 6B, 622 and Matsumoto; fig. 6).

Allowable Subject Matter

8. Claims 1-8, 10 and 11 are indicated to contain allowable subject matter.

9. Claims 31, 32, 33, 38-39, and 45-46 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


CHIEH M. FAN
SUPERVISORY PATENT EXAMINER


Jason M. Perilla
November 28, 2007